LC-AE 00105 LCE

LC AG 00103 POD

RDC

ROCKWELL DESIGN CENTER

R6502-R65C02 PERSONALITY SET FOR LOW COST EMULATOR (LCE) AND RDC MAINFRAME SYSTEM

HARDWARE INSTALLATION MANUAL

Rockwell International

Document No. 29655N10
Order No. RDC10
Rev. 1, December 1984

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Rockwell International

Semiconductor Products Division

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WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to subject J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

INFORMATION TO USER

If this equipment does cause interference to radio or television reception which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- o reorient the receiving antenna
- o relocate the computer with respect to the receiver
- o move the computer away from the receiver
- o plug the computer into a different outlet so that the computer and receiver are on different circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve Radio and TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-0345-4.

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SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The R65O2-R65CO2 Personality Set, in conjunction with the Rockwell Design Center (RDC) Mainframe System (hereafter referred to as the RDC) or the Low Cost Emulator (LCE), emulates the Rockwell R65OO and R65COO family of microprocessors and provides for either isolated or in-circuit testing and debugging of computer programs written for execution on the target microprocessor.

Different models of the personality set provide the target microcomputer adapter/emulator device, emulator probe and cable assemblies to support the various R65O2-R65CO2 microprocessor devices. This manual describes the R65O2-R65CO2 Personality Set and explains how each set is configured to operate with the supported microprocessor and development systems (the RDC and LCE).

1.2 R65O2-R65CO2 PERSONALITY SET FEATURES

- Supports various R65O2-R65CO2 microprocessors with different emulator devices and probe/cable assemblies
- Real-time in-circuit emulation up to 4 MHz
- Five hardware breakpoints with two SYNC outputs for oscilloscope or logic analyzer triggers
- User-defined input for external break signal
- Single-step through interrupts
- User or system supplied power and clock
- Power down capability
- Supports optional 8k/32k/64k byte target RAM for emulation
- Supports full 64k-byte address range for user in prototype or target environment
- ROM-based debug monitor and assembler (LCE)
- Disk-based debug monitor and macro assembler (RDC Mainframe System)
- Menu driven Softkey command selection
- No zero page address conflicts between user and system
- RAM write protection/detection on 16-byte boundaries

1.3 R6502-R65C02 PERSONALITY SET COMPONENTS

Each R6502-R65C02 Personality Set includes a Personality Module Controller (PMC) with interconnect cable set, two enclosed Emulator Pod Modules (EPM), four microprocessor Emulator Devices, two In-circuit Emulation Probes, five configuration jumper headers and interconnecting cables. One personality set version (without PMC and interconnect cable set) supports installation in an LCE while the other version (with PMC and with interconnect cable set) supports installation in an RDC. Figure 1-1 shows a typical R6502-R65C02 Personality Set, identifies the hardware components of the set and shows the physical relationships between the components.

The PMC module has essentially three independent busses: system bus, target bus and emulation bus. The system bus provides the control interface port for the PMC module. The system CPU in the RDC or LCE, which controls the system bus, has complete supervisory control over all PMC operations. The target bus is a separate bus from the system bus controlled by the emulator CPU in the Emulator Pod Modules, with all interaction between these busses performed by the PMC module, under control of RDC or LCE system software. Both the system and target busses are connected to the PMC module through the DIN connectors on the bottom edge of the PMC module. This module is installed in the double-width slot of the system/target bus on both the RDC mainframe and LCE. The emulation bus transfers the R6502-R65C02 device control signals from the Emulation Pod into the PMC module.

The Emulator Pod Modules consist of two interfaces: emulation bus (to PMC module), and user prototype emulation bus. The emulation bus connects the R6502-R65C02 microprocessor within the Emulator Pod Modules to the PMC module. The bus is connected to the PMC module by two ribbon cables. A 60-conductor cable interfaces the PMC to Emulator Pod Module No. 1 (EPM-1) and a 50-conductor interfaces the PMC module to Emulator Pod Module No. 2 (EPM-2). EPM-1 and EPM-2 are mounted in a housing assembly (i.e., pod) and are interconnected by a short 60-pin ribbon cable and a 6-wire power cable. The user prototype emulation bus carries the R6502-R65C02 microprocessor signals to the Prototype-to-Pod Interface Cable which is installed in the target CPU socket.

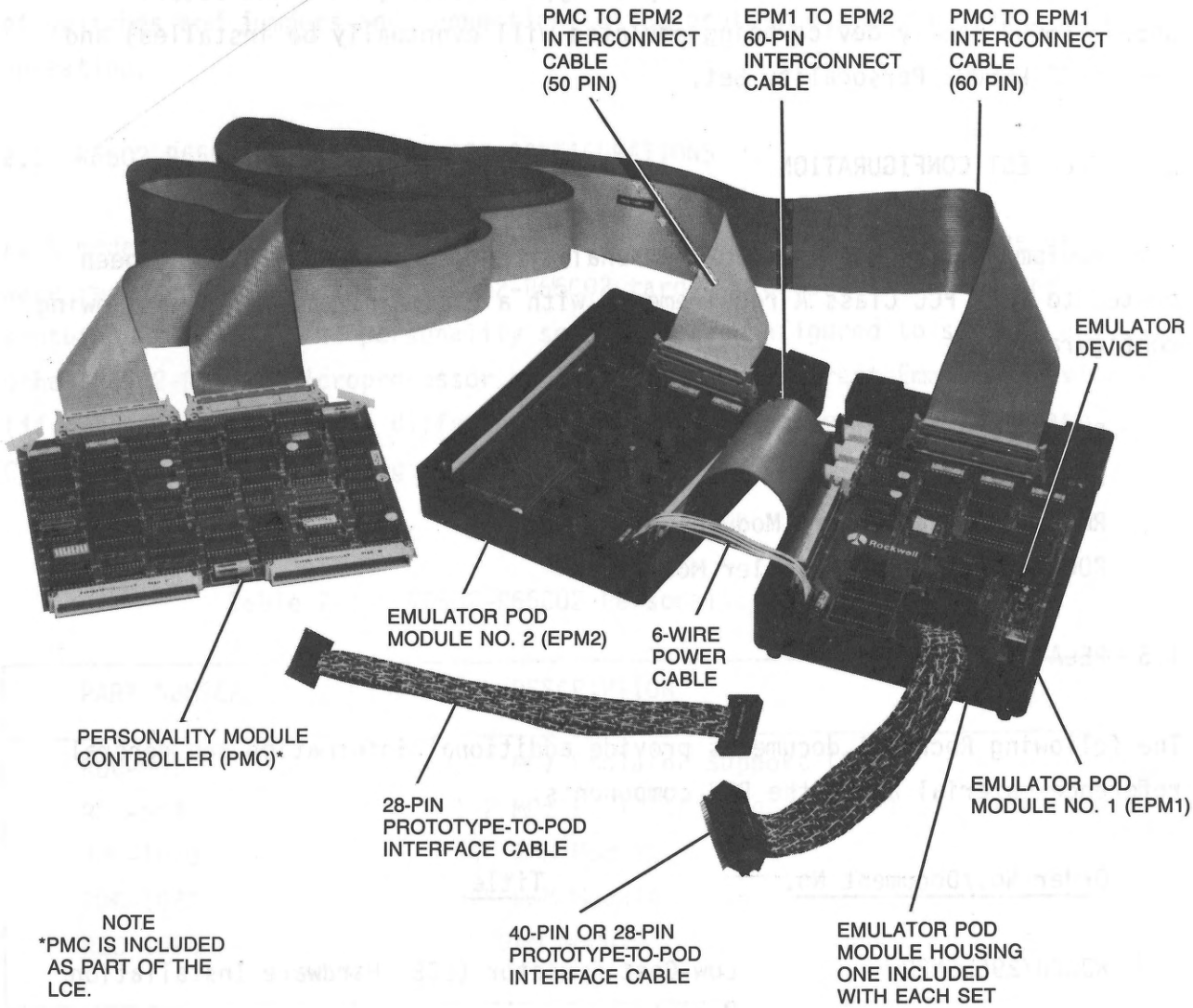

PMC TO EPM2 INTERCONNECT CABLE (50 PIN)
EPM1 TO EPM2 60-PIN INTERCONNECT CABLE
PMC TO EPM1 INTERCONNECT CABLE (60 PIN)
EMULATOR DEVICE
EMULATOR POD MODULE NO. 2 (EPM2)
6-WIRE POWER CABLE
PERSONALITY MODULE CONTROLLER (PMC)*
28-PIN PROTOTYPE-TO-POD INTERFACE CABLE
EMULATOR POD MODULE NO. 1 (EPM1)
NOTE
*PMC IS INCLUDED AS PART OF THE LCE.
40-PIN OR 28-PIN PROTOTYPE-TO-POD INTERFACE CABLE
EMULATOR POD MODULE HOUSING ONE INCLUDED WITH EACH SET

Figure 1-1. Typical R6502-R65C02 Personality Set Hardware Components

The Emulator Device is the device for the particular microprocessor to be emulated which plugs into the EPM-1.

The Prototype-to-Pod Interface Cable consists of a 40-pin or 28-pin ribbon cable connected to a socket on the EPM-1. The opposite end of this cable assembly plugs into the microprocessor socket in the prototype circuitry and provides the interface between the prototype circuit (where the actual R6502-R65C02 family device being emulated will eventually be installed) and the R6502-R65C02 Personality Set.

1.4 FCC TEST CONFIGURATION

This equipment (the R6502-R65C02 Personality Set, model RDC-3101) has been tested to meet FCC Class A requirements with a RDC mainframe in the following configuration:

RM65 SBC Module
RM65 ACIA Module
RM65 Universal Memory Module
RDC Personality Controller Module

1.5 RELATED DOCUMENTS

The following Rockwell documents provide additional information and general reference material about the RDC components.

Order No./Document No.	Title
RDC20/29655N20	Low-Cost Emulator (LCE) Hardware Installation Manual
RDC19/29655N19	Low-Cost Emulator (LCE) System User's Manual
RDC01/29655N01	RDC System User's Manual
RDC16/29655N16	Target RAM Module Installation Manual
201 /2965ON31	R6500 Hardware Manual
202A/2965ON30A	R6500 CPU Programming Manual

SECTION 2

INSTALLATION

The R65O2-R65CO2 Personality Set is shipped ready for integration into an RDC or LCE system. Installation is easy, involving a few simple steps, and requires only a screwdriver to complete. Setup requires only the positioning of switches and jumpers and connection to the prototype circuit before operation.

2.1 R65O2-R65CO2 PERSONALITY SET CONFIGURATIONS

Each model listed in Table 2-1 is complete, i.e., it contains all the hardware required to emulate the R65O2-R65CO2 target microprocessors in the prototype circuit. The personality set can be reconfigured to support any other R65O2-R65CO2 microprocessor by installing a different Emulator Device (if needed), connecting a different in-circuit Prototype-to-Pod Interface Cable (if needed) and changing jumper headers (if needed).

Table 2-1. R65O2-R65CO2 Personality Set Modules

PART NUMBER	DESCRIPTION
RDC-502	1-2 MHz Emulator Support (RDC)
RDC-509	1-2 MHz Emulator Support (LCE)
RDC-1020	64K RAM Module
RDC-1022	32K RAM Module
RDC-1024	8K RAM Module

There are five Emulator Devices. Each device supports a group of R65O2-R65CO2 microprocessors and consists of the emulator microprocessor device for that group that plugs into EPM-1. Table 2-2 lists the Emulator Devices.

There are two different cables that connect the microprocessor being emulated to the Emulator Device. Table 2-3 lists these cables for the compatible Emulator Device(s).

Table 2-3 is a matrix for determining the Emulator Device, Prototype-to-Pod Interface cable and jumper header required to configure the R6502-R65C02 Personality Set for emulating different R6502-R65C02 microprocessors. The jumper headers are only used when emulating the 28-pin devices. To use the table, locate the device you wish to emulate in the EMULATED DEVICE column. The two columns to the right of the EMULATED DEVICE column identify what is needed to configure the R6502-R65C02 Personality Set for the microprocessor you want to emulate.

2.2 COMPONENT CHECKLIST

Each R6502-R65C02 Personality Set consists of the same basic components which are listed in Table 2-4. While checking each component, look for any indication of damage during shipment. If any connector pins are bent, carefully straighten them. Look also for any possible damage to the Emulator Pod Module Housing assembly (the black enclosure) such as broken edges or something loose when shaken.

Table 2-2. Emulator Device Models

PART NUMBER	DESCRIPTION
R6502	Emulator Device for the R6502, R6503, R6504, R6505, R6506 and R6507 devices.
R6512	Emulator Device for the R6512, R6513, R6514 and R6515 devices.
R65C02	Emulator Device for the R65C02 devices.
R65C102	Emulator Device for the R65C102 devices.*
R65C112	Emulator Device for the R65C112 devices.*

*Note: These emulators are supplied only upon order by the user.

Table 2-3. Configuration Matrix

EMULATED DEVICE	REQUIRED PROTOTYPE-TO-POD INTERFACE CABLE	JUMPER HEADER
R6502	40-pin	---
R6503	28-pin	001
R6504	28-pin	001
R6505	28-pin	011
R6506	28-pin	021
R6507	28-pin	011
R6512	40-pin	---
R6513	28-pin	031
R6514	28-pin	031
R6515	28-pin	041
R65C02	40-pin	---
R65C102	40-pin	---
R65C112	40-pin	---

Table 2-4. Component List

QUANTITY	ITEM	DESCRIPTION
1	*PMC Module	Controller module that plugs into the RDC mainframe or LCE.
2	*PMC to Pod Interface Cables (Long Length)	One ribbon cable with 60-pin connector each end and one ribbon cable with a 50-pin connector on each end.
1	Emulator Pod Module Assembly	Pod that contains EPM-1 and EPM-2, a short ribbon cable, a six-wire power cable, and the R6502 Emulator Device.
1	Emulator Package	Package contains the R6512, R65C02, R65C102 and R65C112 Emulator Devices and 5 jumper headers for the 28-pin processors.
2	Probe-to-Pod Interface Cables (Medium Length)	One ribbon cable with 40-pin connectors on each end. Used for emulating the R6502, R6512, R65C02, R65C102 or R65C112. One cable with a 28-pin connector on each end. Used for emulating the R6503, R6504, R6505, R6506, R6507, R6513, R6514 or R6515.

* These components are not included in the RDC-509 version because they are factory installed as part of the LCE system.

2.3 INSTALLATION OF THE PERSONALITY SET

The Personality Set is shipped with the Emulator Pod Modules and PMC module (RDC) pre-configured for the family of R650X, R651X, R65C02, R65C102, and R65C112 devices. This section describes the procedure for checking out the configuration and then installing all of the properly configured Personality Set pieces.

2.3.1 Checking the Configuration of the PMC Module

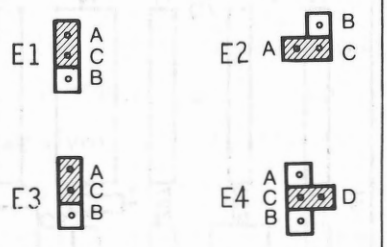
With the PMC module removed from its mainframe, check the configuration of jumpers and switches on the PMC module against those shown in Table 2-5 (the factory settings). If any of the settings are different than Table 2-5, change them to agree with the table. When properly configured, install the PMC Module in the mainframe.

Table 2-5. PMC Module Jumpers and Switch Configurations

JUMPERS CONFIGURATION

E1	E2	E3	E4
A	A	A	C

LEGEND FOR JUMPERS



PMC	Z10 SWITCH CONFIGURATION							
TARGET ID	1	2	3	4	5	6	7	8
0	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	OPEN	CLOSED	CLOSED
1*	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
2*	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	OPEN	OPEN	CLOSED
3*	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	OPEN	OPEN	OPEN

NOTE:

The LCE and RDC use Target ID #0 as the standard ID.

Target ID addresses 1, 2, and 3 are only available on the RDC Mainframe and are intended as alternate ID addresses.

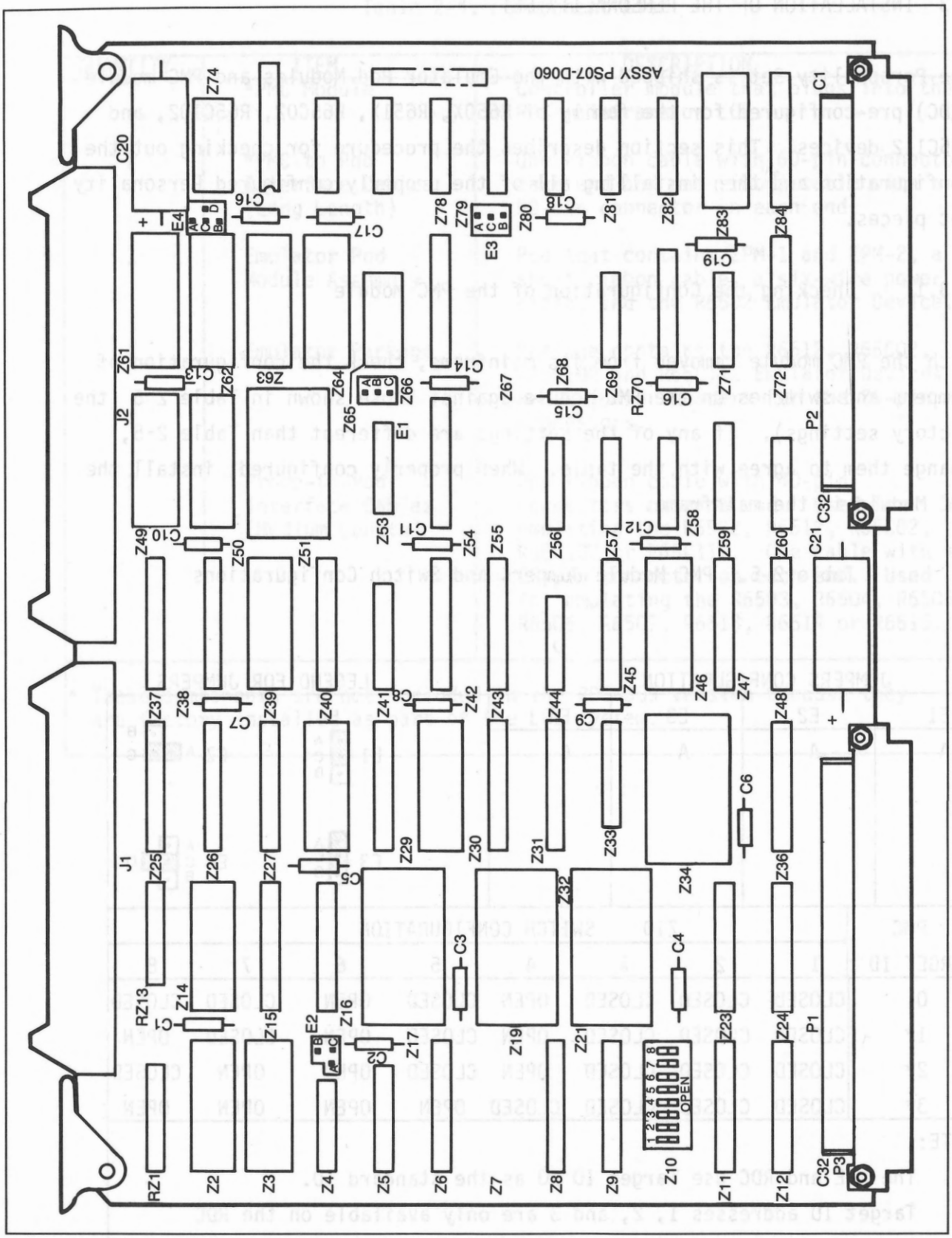


Figure 2-1. PMC Module Jumper and Switch Locations

2.3.2 Configuring the 8K/32K/64K Target RAM Module

The 8K/32K/64K Target RAM module is set the same for all R6502-R65C02 devices. The jumper settings and switch positions are described in the Target RAM Module Installation Manual.

2.3.3 Interconnection of the Personality Set

Position the PMC module, the two long ribbon cables, and the Prototype-to-Pod Interface Cable. Figure 2-2 shows the correct orientation of the different components.

In the following procedures, pay close attention to the pin orientation when mating connectors. The printed circuit boards have pin 1 and the last pin of the connector marked on the module. The ribbon cable connectors have pin 1 identified by an arrow [▲], a notch, and/or the number 1. Failure to correctly orient the cable on the connector may result in damage to the printed circuit board when power is applied.

Connect the PMC module to the EPM using the following procedure:

a. RDC only. Locate the shielded cable clamps. The cable clamps should be mounted at the front and the rear of the RDC mainframe card cage. Loosen the cable clamping screws with a screwdriver. Route the two long cables from the EPM through the slotted opening at the front or back of the RDC mainframe and through the respective cable clamp. Pull the cable through until the exposed shield area is inside the cable clamps. Tighten the clamp by tightening the cable screws snuggly.
b. Connect the free end of the 60-pin (the other end should be connected to the PMC at connector J2), long ribbon cable to the connector on the EPM-1 marked J1.
c. Properly seat the connector.
d. Connect the free end of the 50-pin (the other end should be connected in the PMC at connector J1), long ribbon cable to the connector on the EPM-2 marked J1.
e. Seat the connector properly and snap the connector retainers in place.

2.3.4 Inserting the Prototype-to-Pod Interface Cable into Prototype

Make certain that the main power switch to the prototype system is off and insert the free end of the Prototype-to-Pod Interface Cable into the device socket where the device to be emulated would normally be installed. Use extreme care when plugging the probe into the socket to insure that no pins are bent or misaligned.

This completes the installation of the R6502-R65C02 Personality Set into the RDC or LCE and the prototype system.

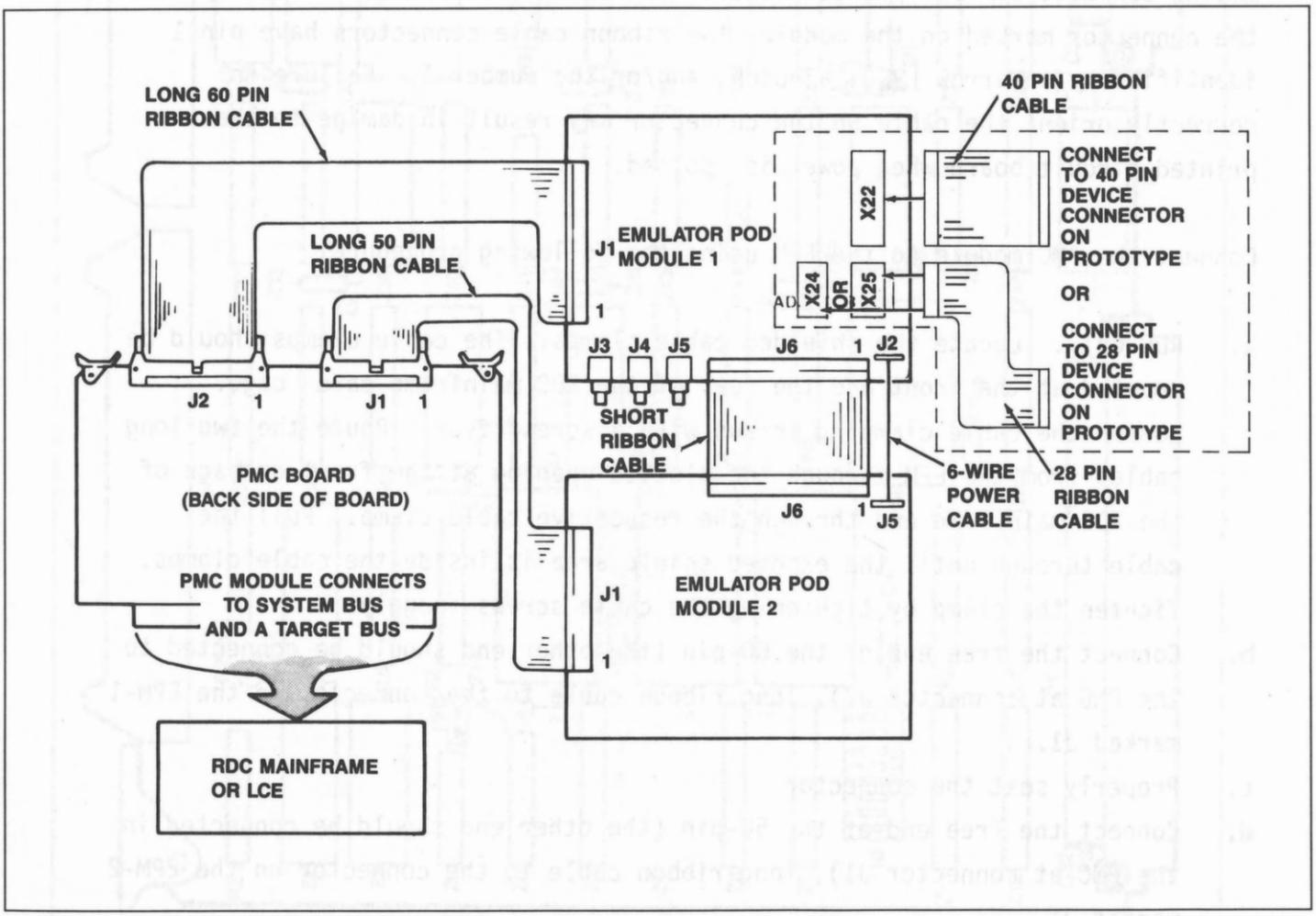


Figure 2-2. Ribbon Cable Interface Connections

2.4 MICROPROCESSOR DEVICE EMULATION

This section describes the addressing modes and memory map of the various R6502-R65C02 devices including R6502, R6503, R6504, R6505, R6507, R65C02, R65C102, R65C112, R6512, R6513, R6514 and R6515.

Prototype Memory	This is a memory or I/O which is physically in the prototype, addresses through the interface cable. Typically this memory is the same as is used in the final application.
Target Memory	This is memory which is physically in the target bus. Typically this memory is available at emulation time only, and not present in the actual application except for simulating prototype memory.

2.4.1 R65XXX 64K Device

Figure 2-3 shows the memory map of the R65XXX 64K Emulator Device. The features of the memory map are described below.

Emulation RAM	Since there is 64K bytes available to the prototype, the full memory map can be used as emulation RAM.
8K/32K/64K RAM Module	The entire 64K block of memory is available on the target bus for simulation purposes when using the RAM module with 64K option.
SYSGEN memory	Target memory is available from $0000-$FFFF Prototype memory is available from $0000-$FFFF.

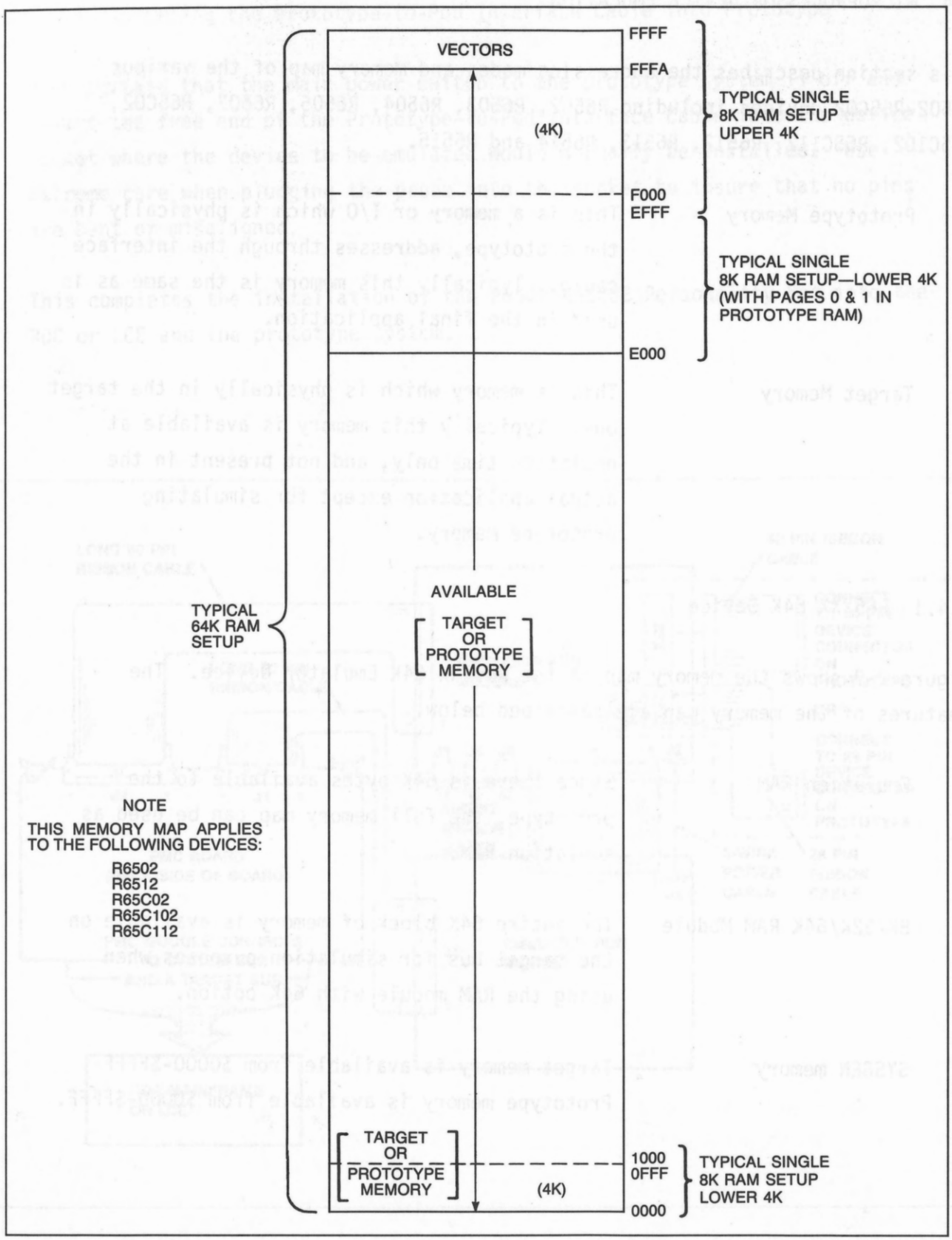


Figure 2-3. R65XXX 64K Device Memory Map

2.4.2 R65XXX 8K Devices

Figure 2-4 shows the memory map of the R65XXX 8K device. The features of the memory map are described below.

Emulation RAM	This 8K block of memory $0000-$FFFF is available on the target bus for emulation of prototype memory. Only this area is unique in the prototype.
8K/32K/64K RAM Module	The entire 64K block of memory is available on the target bus for emulation purposes when using the target RAM module with 64K option. The actual emulation memory area is located from $0000 to $1FFF.
SYSGEN memory	Target memory is available from $0000-$FFFF. Prototype memory is available from $0000-$1FFF. Memory beyond this range is redundantly mapped. Note: Emulation code must originate at two locations for valid execution. The upper 4K must be at $F000 to $FFFF to provide support for vectors located at $FFFA to $FFFF. The lower 4K must originate at $0000 to $0FFF.

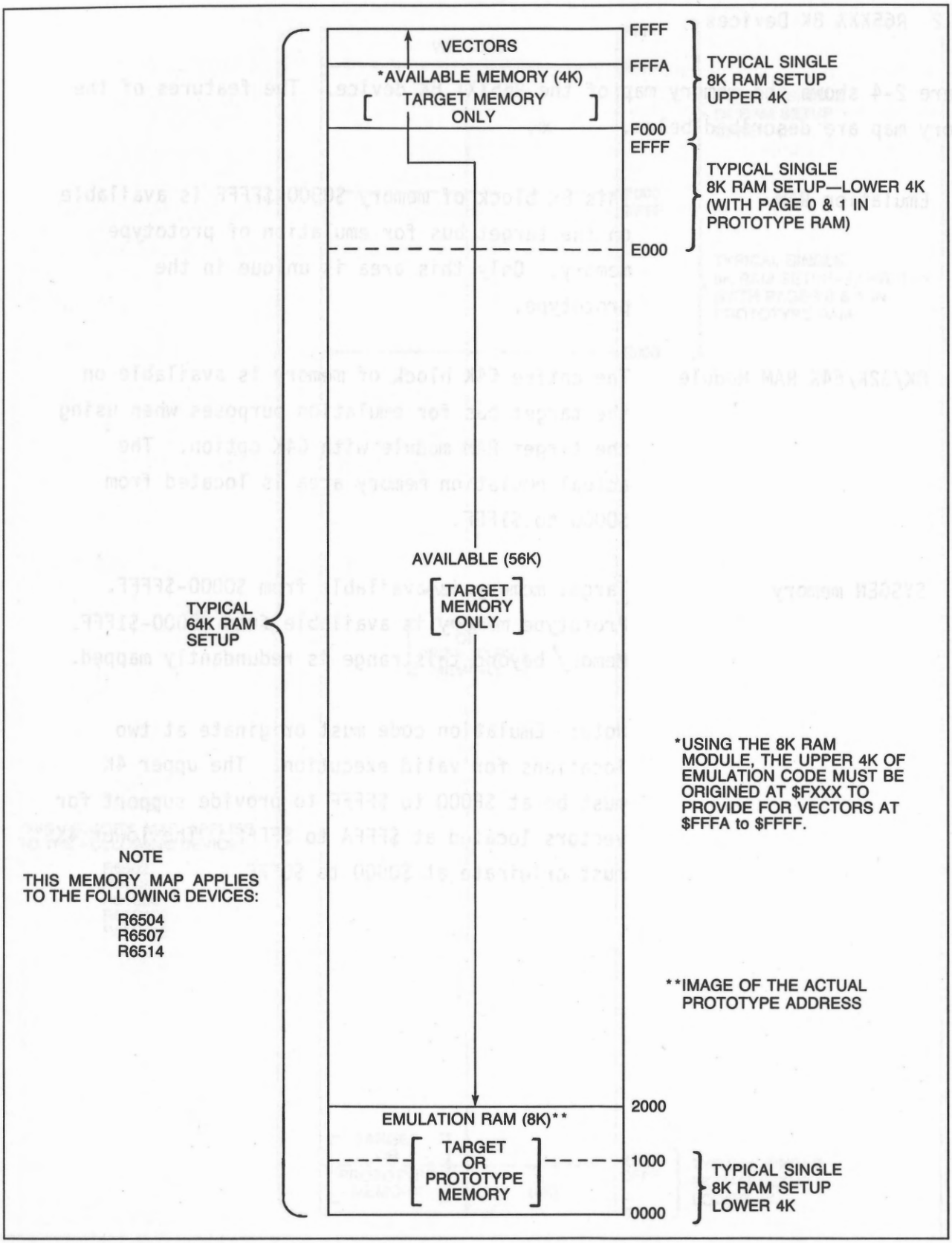


Figure 2-4. R65XXX 8K Device Memory Map

2.4.3 R65XXX 4K Device

Figure 2-5 shows the memory map of the R65XXX 4K device. The features of the memory map are described below:

Emulation RAM	This 4K block of memory $0000-$0FFF is available on the target bus for emulation of prototype memory. Only this area is unique in the prototype.
64K RAM Module	The entire 64K block of memory is available on the target bus for emulation purposes when using the RAM module with 64K option. The actual emulation RAM is located from $000 to $0FFF.
SYSGEN memory	Target memory is available from $0000-$FFFF. Prototype memory is available from $0000-$0FFF. Memory beyond this range is redundantly mapped.

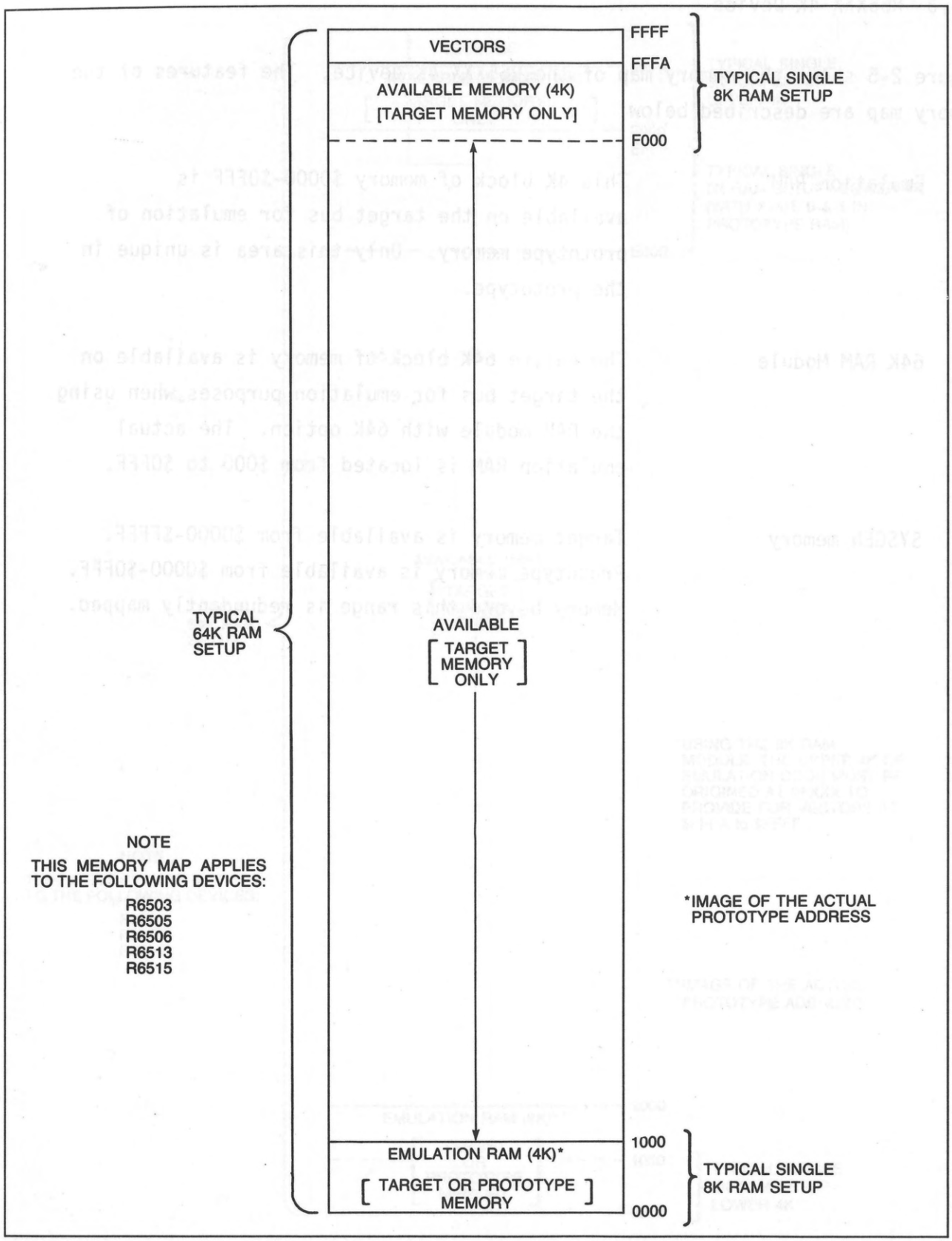


Figure 2-5. R65XXX 4K Device Memory Map

2.5 RECONFIGURING THE PERSONALITY SET

If the Personality Set is to be changed to emulate another microprocessor device, the EPM must be reconfigured as described in the following section.

2.5.1 Reconfiguring the Emulation Pod

a. Position the Emulator Pod Housing Assembly so that the top label can be read.
b. Remove the four screws from the bottom of the housing.
c. Holding the housing, open the two halves like a book, keeping the back edges close together so that the short ribbon cable and the power cable connecting the two EPM modules are not disconnected.
d. Lay the two halves of the housing down so that the EPM-1 (board with CPU) is above EPM-2 as shows in Figure 2-6. The component locations should be readable on both EPM modules.
e. There are 9 jumpers on the EPM-1 module identified as E1 through E9. Table 2-6 defines the settings for each configuration. The type of emulator is across the top row. Below each emulator type entry is the position of each of the 9 jumpers, used to select options. The JUMPER OPTIONS row in the table explains the settings for each jumper.
f. Locate the jumper E1 on EPM-2. Configure jumper E1 so that the power-down detection circuitry will be supplied with +5V from either a user supplied source or from the RDC mainframe or LCE as required. Table 2-7 defines the settings for this jumper.
g. Locate the Device Adapter (ZIF connector), marked XZ1 on EPM-1 module, and insert the Emulator Device for the device to emulate. Pin 1 is located at the corner nearest the locking lever of the Device Adapter (ZIF) and is also silkscreened on EPM-1. Table 2-8 shows the part number for the device to be emulated and the corresponding Emulator Device, and (if required) the appropriate jumper header.

NOTE

The lever in the lower right corner of the Device Adapter must be in the up position to insert the Emulator Device. Lower the lever after the Emulator Device is properly seated.

h. Insert the proper jumper header at location XZ3 on the EPM-1 module.

NOTE

The on-board oscillator circuit is factory configured with a crystal which allows an operating frequency of one half or one quarter of the frequency of the crystal (Y1). Other operating speeds may be achieved by changing Y1. The oscillator circuit will operate within a crystal frequency up to 16 MHz. The second crystal (Y2) is used to operate with the R65C102 and can also be changed for different operating speeds of this device.

This completes the emulator configuration procedure. Check that the ribbon cable and power cable connecting the two EPM modules are properly seated on their respective connectors.

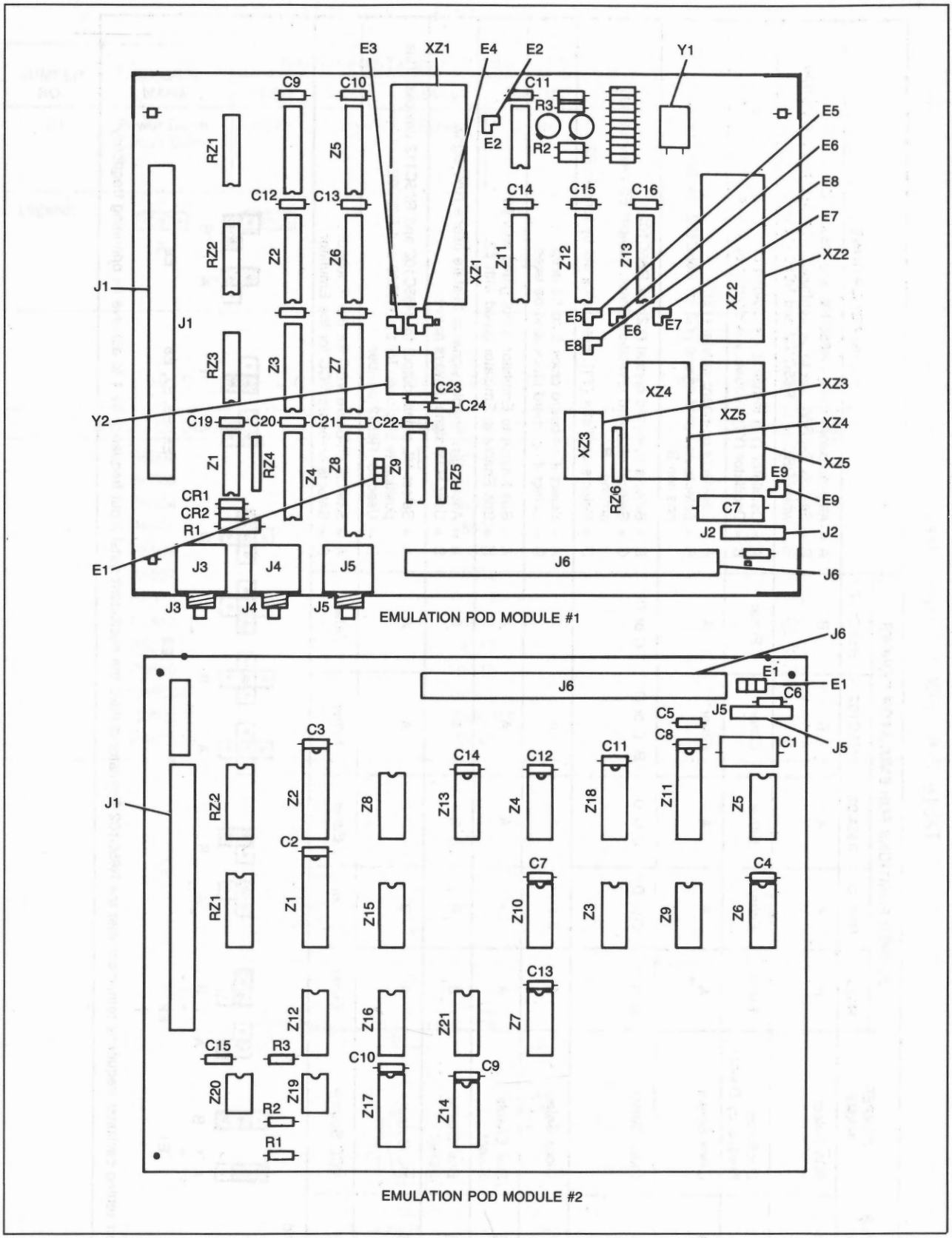
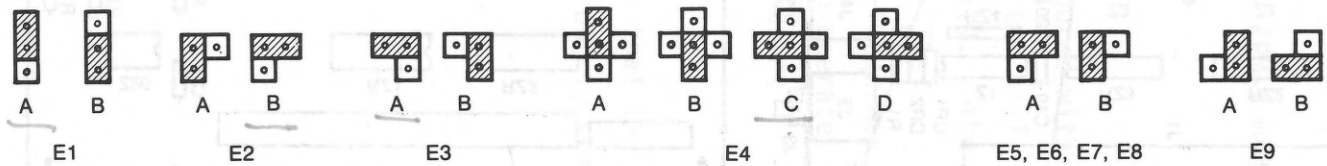


Figure 2-6. EPM Modules Jumper Locations

Table 2-6. EPM-1 Jumper Matrix

JUMPER NO.	JUMPER NAME	JUMPER POSITIONS FOR EMULATOR DEVICES					JUMPER OPTIONS
		R6502	R6512	R65C02	R65C102	R65C112	
E1	R/$\overline{W}$ Select	A	A	A	B	B	A = All processors except R65C102 and R65C112. B = Selects the R/$\overline{W}$ line to be controlled from the user's prototype when DBE = L. R65C102 and R65C112 only.
E2	Oscillator Frequency Divider	Either	Either	Either	Either*	Either	A = Oscillator (Y1) frequency is divided by 2 (÷2). B = Oscillator (Y1) frequency is divided by 4 (÷4).
E3	Clock Select	A	A	A	Either*	A	A = Deselects on-board crystal (Y2). B = Selects on-board crystal (Y2) for R65C102. E4 must be in position B.
E4	Clock Select	C or D	C or D	C or D	B, C or D	C or D	B = Selects on-board crystal (Y2) for R65C102. C = Selects off-board crystal/oscillator. Jumper E2 recommended setting—B. D = Selects oscillator (Y1). Frequency set by jumper E2.
E7	Clock Select Ø1	A	Either	A	A	A	A = Select if off-board clock is to be used. B = Select if on-board clock is to be used.
E5	Bus Enable Select	A	A	A	A	A	A = Bus Enable to Emulator is not gated with Ø2. B = Bus Enable to Emulator gated with Ø2.
E8	Bus Enable Select	B	B	B	A	A	A = Allows Bus Enable signal to tri-state user's R/$\overline{W}$ signal. B = User R/$\overline{W}$ signal always active.
E6	$\overline{ML}$ Output	A	B	A	A	A	A = Select $\overline{ML}$ signal output for R65C102 and R65C112 devices. This position is also used for the R6502 and R65C02. B = Used for R6512 devices.
E9	VCC Source	Either	Either	Either	Either	Either	A = Selects off-board VCC for the Emulator. B = Selects on-board VCC for the Emulator.

Legend:



*When setting oscillator frequency remember that the R65C102 Emulator divides the oscillator/crystal input frequency by 4 to achieve its operating frequency.

Table 2-7. EPM-2 Jumper Matrix

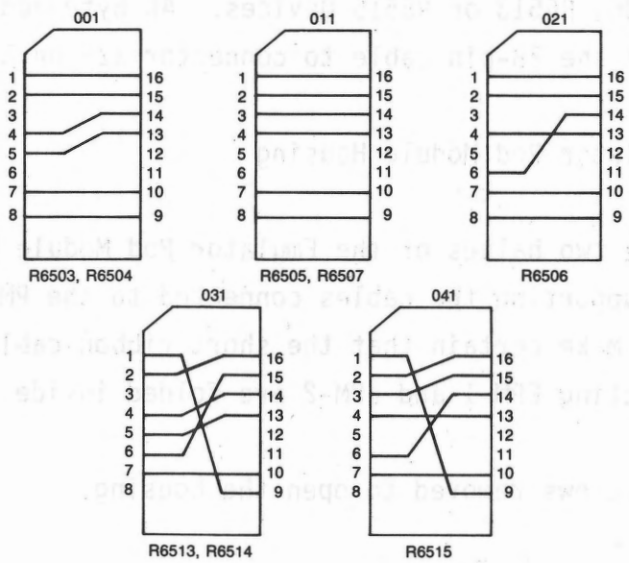
JUMPER NO.	JUMPER NAME	JUMPER POSITIONS FOR EMULATOR DEVICES					JUMPER OPTIONS
		R6502	R6512	R65C02	R65C102	R65C112	
E1	Power Down Circuit Select	Either	Either	Either	Either	Either	A = User power used as input to power down detect. B = MTDS or LCE power used as input to power down detect.

Legend:

E1

Table 2-8. Jumper Header Matrix and Jumper Configuration

EMULATED DEVICE	EMULATOR DEVICE	JUMPER HEADER
R6502	R6502	none
R6503	R6502	001
R6504	R6502	001
R6505	R6502	011
R6506	R6502	021
R6507	R6502	011
R6512	R6512	none
R6513	R6512	031
R6514	R6512	031
R6515	R6512	041
R65C02	R65C02	none
R65C102	R65C102	none
R65C112	R65C112	none



2.5.2 Connecting the Prototype-to-Pod Interface Cables to EPM-1

In the following procedures, pay close attention to the pin orientation when mating connectors. The printed circuit boards have pin 1 and the last pin of the connector marked on the module. The ribbon cable connectors have pin 1 identified by an arrow [▲], a notch, and/or the number 1. Failure to correctly orient the cable on the connector may result in damage to the printed circuit board when power is applied.

Connect one end of the Prototype-to-Pod Interface Cable to the EPM-1 module in one of three methods listed below:

NOTE

In the following steps, refer to Figure 2-6 for location of the connectors on the EPM-1 boards. Table 2-9 summarizes these steps.

a. R6502, R6512, R65C02, R65C102 or R65C112 Devices. 64K byte addressable memory. Connect one end of the 40-pin cable to connector XZ2 on EPM-1.
b. R6504, R6507 or R6514 Devices. 8K byte addressable memory. Connect one end of the 28-pin cable to connector XZ4 on EPM-1.
c. R6503, R6505, R6506, R6513 or R6515 Devices. 4K byte addressable memory. Connect one end of the 28-pin cable to connector XZ5 on EPM-1.

2.5.3 Closing the Emulator Pod Module Housing

a. Carefully fold the two halves of the Emulator Pod Module Housing together, while supporting the cables connected to the PMC and In-circuit Emulation Probe. Make certain that the short ribbon cable and 6-wire power cable connecting EPM-1 and EPM-2 are folded inside the housing and not pinched.
b. Replace the four screws removed to open the housing.

Table 2-9. Prototype-to-Pod Interface Connection to EPM-1

DEVICE EMULATION	CABLE TYPE	EPM-1 CONNECTION SOCKET
R6502, R6512, R65C02 R65C102, R65C112	40-pin	XZ2
R6504, R6507 or R6514	28-pin	XZ4
R6503, R6505, R6506, R6513 or R6515	28-pin	XZ5

SECTION 3

DEBUG SYSTEM FUNCTIONAL DESCRIPTION

Operation of the RDC or LCE with the R65O2-R65CO2 Personality option is similar to the operation of the RDC or LCE in standalone mode except that there are at least two CPU's.

This section also presents a functional description of specific elements of the R65O2-R65CO2 Personality Set as they apply to the Debug System and its operation. The actual operating commands are provided in the RDC System User's Manual, or LCE System User's Manual.

3.1 R65O2-R65CO2 DEBUG OPERATIONS

The R65O2-R65CO2 Debug software provides the following operations and features for all targets under control of the RDC or LCE:

Target Memory functions

- Show and alter memory - Any target memory location may be displayed and altered including ASCII text entry and display.
- Disassembly of target memory
- Load, save or verify of target memory

Target CPU Register functions

- Load and save to/from disk (RDC only).
- Load and save to/from host system.
- Show and alter any register - Any of the six registers may be displayed and altered.

Target Breakpoints

- Set hardware breakpoint - Hardware breakpoints may be set to interrupt program on any instruction fetch, write/read, or access of a particular data value from a particular memory location in the range of $0000 to $FFFF. If the breakpoint 1, or breakpoint 2 are set up, a scope sync pulse, (scope sync 1 or scope sync 2) is provided at the rear of the Emulator Pod Module Housing assembly for a real-time debugging with an oscilloscope.
- External Breakpoint (HALT) - The HALT input to the emulator pod is an active low input which is used to externally halt the emulator.

Target Run

- Two modes of operation - Single-step (step) and Real-time (normal) Execution

    1. Single-step execution Mode
        - Execution is non-real time.
        - Tracing of each instruction can be performed with symbolic disassembly.
        - Up to five breakpoints can be set.

Single-step mode - The single step mode allows close control of the program. A count field is provided to step the processor from one to 9999 instruction steps. Capability is also provided to step forever [9999], with the ability to interrupt the program via the ESCAPE key.

    2. Real-time execution Mode
        - R6502-R65C02 microprocessor is executing at full speed
        - Execution proceeds until halted by the user or a breakpoint is encountered.
        - A breakpoint/matchpoint definition can be entered or modified while the microprocessor is executing, including scope sync to be changed.
        - RESET can be performed within the prototype allowing program to be restarted.

Target Reset

- Same features as RUN except it begins execution with a hardware reset.
- A configured Debug reset is provided.
- Step capability through user RESET with symbolic disassembly.

Protection of Target Memory

- Write protect or unprotect any segment(s) of Target RAM.
- Access to a protected area causes a breakpoint.

Directory of the Disk (RDC only)

- Displays or lists the directory contents of any diskette.

Additional Features

- $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$ vectors - The $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$ vectors are not used for breakpoint conditions. The user has complete control over these vectors.
- I/O device flexibility - Target memory operations may be from or to any RDC or LCE system device.
- Proper memory check - the system checks for attempts to modify non-existent or read-only memory and will indicate a fault.
- Allows use of prototype RAM to replace/supplement.

3.2 FUNCTIONAL DESCRIPTION

The R6502-R65C02 Personality Set option for the RDC and LCE consists of a module controlling its own Emulator Pod Modules and In-circuit Emulation Probe for a specific R6502-R65C02 microcomputer device. Up to four of these personality sets can be installed within the RDC mainframe. The PMC modules used in the personality sets are differentiated by which RM65 target bus they are plugged into, and the switch settings of Switch Bank Z10 on the PMC module. The LCE supports a single personality set.

3.2.1 Memory Control

The system bus and the R6502-R65C02 Personality Sets all run asynchronous with respect to each other, allowing 1 to 4 MHz devices to be tested together within the RDC or LCE. Each Personality Set can use an optional 8K/32K/64K module as target memory to replace memory external to the target system. The 8K/32K/64K RAM modules is used only when the user's program is executing out of the target RAM instead of the prototype memory. The 8K/32K/64K or 64K block of memory as well as prototype target memory are accessed by the RDC or LCE system bus through the PMC.

3.2.2 Hardware Breakpoints

The hardware breakpoint trigger with a 16-bit address, 8-bit data with mask, and control data (i.e., instruction fetch, read operation, write operation, $\overline{\text{NMI}}$, or $\overline{\text{IRQ}}$). Once a break condition has been satisfied, an active low strobe with a minimum duration of one clock cycle is generated and available on the SYNC 1 and 2 BNC connectors at the rear of the Emulation Pod Module Housing assembly (these triggers are delayed 1 emulator CPU clock cycle). Also, if the breakpoint is to cause a Halt condition, this strobe also causes an $\overline{\text{NMI}}$ break to be initiated, which halts the target CPU.

The $\overline{\text{NMI}}$ break signal is strobed into the Emulator Pod Module during the Sync pulse (instruction fetch cycle). At the instruction fetch, the Emulator Pod Module logic forces a continuously repeating JMP sequence onto the emulator's data bus, putting the target microprocessor into a Halt or suspended state.

a. Case 1: If a Hardware Breakpoint occurs due to an op code fetch, (qualified with Sync), an $\overline{\text{NMI}}$ break is generated at I. (See Figure 3-1). The address and the disassembled instruction are displayed in the following order:
   (1) The address and instruction prior to the breakpoint match.
   (2) Address of instruction where the breakpoint match occurred.
   (3) Address of instruction last executed.
   (4) Address of instruction to be executed following the break (next PC address).

b. Case 2: If a breakpoint occurs during data or I/O cycle (if this is the last machine cycle of the instruction cycle), the breakpoint is qualified and an $\overline{NMI}$ break is generated at J. (See Figure 3-1). The address and the disassembled instructions are displayed in the following order:
   (1) Address of instruction executing when the breakpoint match occurred.
   (2) Address of instruction executed which follows the breakpoint match.
   (3) Address of instruction last executed.
   (4) Address of instruction to be executed following the break.

c. Case 3: If a breakpoint is generated when an op code fetch (unqualified with Sync) occurs, the presentation of addresses and instructions follows the sequence shown in Case one.

NOTE

Because of the pipeline nature of the 6502 device, care must be taken when a branch instruction precedes the matched instruction. If a sync is not included, a branch may be taken and a dummy cycle generated while the new effective displacement is being computed, causing an incorrect breakpoint.

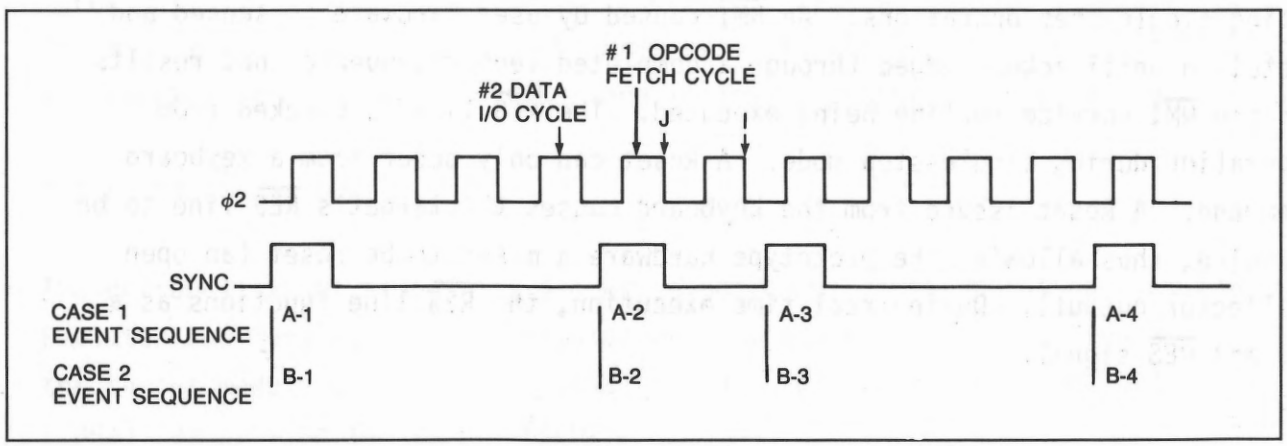


Figure 3-1. Ø2 and SYNC Signal Timing for Breakpoints

d. Case 4: If a breakpoint is generated when an operand fetch occurs, the presentation of addresses and instructions follows the sequence listed in either case one or two depending on the following:

(1) If the operand fetched is in Immediate Addressing Mode, then the presentation follows that shown in Case 2.

(2) All other addressing modes on an operand fetch follow the presentation of a through d shown in Case 1.

There is one externally available input to the emulator pod that is capable of causing a hardware breakpoint on an occurrence of a high to low transition. This input is over-voltage protected a +15 or a -10 volt to 0 volt swing on a 50% duty cycle, +10 or a -5 volt continuous DC level.

The $\overline{\text{NMI}}$ line of the emulator pod is sampled by its CPU during Ø2 clock to ensure that the $\overline{\text{NMI}}$ line functions the same while in emulation as it does in the production device. In order to clear the edge triggering nature of the $\overline{\text{NMI}}$ line, it must be high for at least one Ø2 clock cycle.

3.2.3 Single-Step Mode Control

The $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ and $\overline{\text{RES}}$ interrupts may be controlled through a combination of hardware and software to disable or enable them during single-step operation. The $\overline{\text{IRQ}}$ is controlled separately from the $\overline{\text{NMI}}$ and $\overline{\text{RES}}$ interrupts.

The $\overline{\text{NMI}}$ line is controlled during the single-step mode as a means of generating single-step operations. An $\overline{\text{NMI}}$ caused by user hardware is sensed and retained until acknowledged through a completed vector sequence that results in the $\overline{\text{NMI}}$ service routine being executed. The $\overline{\text{RES}}$ line is blocked from operation during single-step mode. A Reset can only occur from a keyboard command. A Reset issued from the keyboard causes the target's $\overline{\text{RES}}$ line to be toggled, thus allowing the prototype hardware a means to be reset (an open collector output). During real time execution, the $\overline{\text{RES}}$ line functions as a normal $\overline{\text{RES}}$ signal.

3.2.4 Power-Down Mode

The Personality Set supports a power-down situation. If power-down occurs in the RDC or LCE during a non-real-time operation (either during single-step, or when halted with a breakpoint), restart can only occur after power is reapplied with a Reset being issued from the keyboard. This insures that the Debug system is in control of the restart. In real-time execution, power-down is not restricted and breakpoints are operational only after power has been restored and the emulation device has been reset.

Breakpoints (including the external trigger breakpoint) should be set so that they occur after power-up and after the stack pointer has been initialized. If the external trigger breakpoint occurs during real-time running and a power-down is in progress, then a breakpoint occurs as soon as the Reset vector sequence begins executing after a power-on, thus forcing an NMI break sequence. If the Reset sequence results in an unknown register state that may contain an invalid stack pointer, an incorrect program counter or processor status may (in fact most likely will) occur. To avoid this, care should be taken to set breakpoints at program code locations after the stack pointer has been initialized. To avoid this, an external trigger breakpoint should not be allowed to come in during a power-down condition.

3.2.5 Stack Pointer Control

During STEP mode, the stack pointer must point to valid RAM with at least three valid locations following to insure full system control is maintained. The Register Change command can be used prior to the Run command to initialize the stack pointer to a valid RAM range to insure proper Step operation.

3.2.6 Clock Options

The Personality Set allows the jumper selection of clock operation from the Emulator Pod Modules on-board crystal oscillator, external clock source from the target module or on-board crystal as the clock source (R65C102 only, 1 MHz) for driving the R6502-R65C02.

3.2.7 Buffered Lines to the Emulator Pod Module

The address bus, data bus, Ø2 clock, R/$\overline{W}$, and Sync lines are buffered lines.

3.2.8 Zero-Page RAM

The LCE Debug system makes extensive use of the lower 1K of RAM in normal operation. To avoid any conflict with user programs the system keeps a mirror image of the lowest 1K for Z-page and stack RAM data. This image is used to restore the user RAM prior to restart. This image Z-Page RAM is write protected from the user program during all emulation functions.

APPENDIX A

ERROR MESSAGES

Emulator not ready

The emulator device is not functioning properly. The emulator device could be powered down (as in the case when using prototype power for the emulator). The PMC module could be improperly configured, or the PMC could be disconnected from the Personality Set Emulator Pod Module Housing. Another possible cause for this error is that the CPU locked up by attempting to execute an illegal opcode, in which case the emulator should be reset before continuing. Also, if the READY line is low (the emulator's READY line must be high when using the emulator to run debug functions, e. g., memory dump) this error message can appear.

Memory failure at address XXXX, is XX should be XX

The system could not write to target or prototype memory properly. This error will also occur if a modify command is attempted at a write protected address.

Illegal op code error

Emulator CPU tried to execute an op code that is not a valid member of its instruction set. The message indicates that the emulator CPU has been halted and displays the instruction before the illegal op code, the address of the illegal op code, and the instruction executed after the illegal op code.

Write protect error

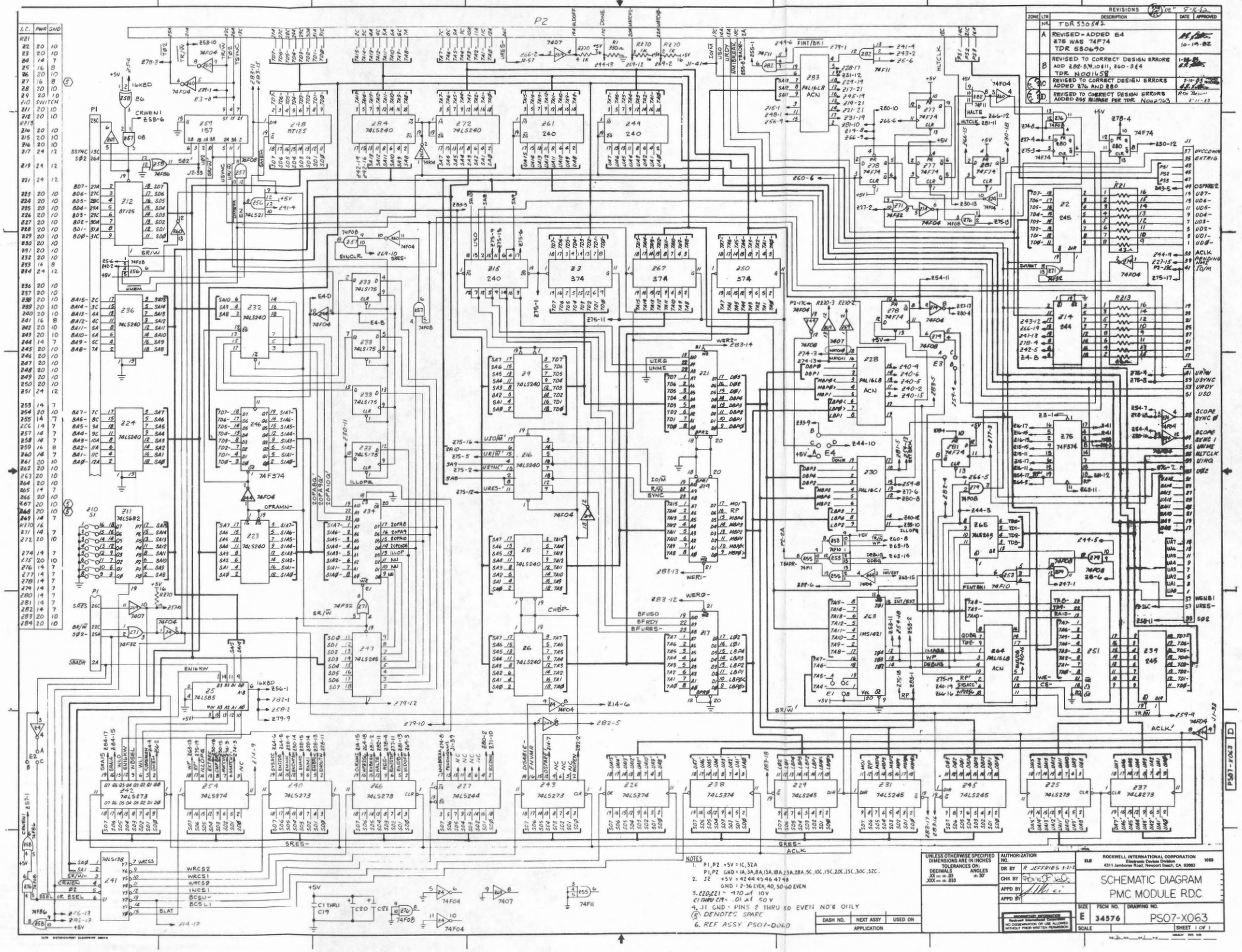
See Section 3 of the LCE System User's Manual or Section 11 (Memory Control) of the RDC System User's Manual (as applicable) for an explanation of user protected memory procedures.

APPENDIX B

SCHEMATIC DIAGRAMS

This appendix contains the schematic diagrams for the personality set modules used with the RDC and LCE systems. These schematic diagrams are presented in this appendix as reference material only and are subject to change without notice if deemed necessary by Rockwell International to improve the product.

Module Name	Drawing No.
Personality Module Controller (PMC)	PS07-X063
R6502-R65C02 Emulator Pod Module Board 1 (EPM-1)	PS07-X036
R6502-R65C02 Emulator Pod Module Board 2 (EPM 2)	PS07-X041


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
NR TDR 530542
A REVISED - ADDED E4 Z76 WAS 74F74 TDR 580690 10-19-82
B REVISED TO CORRECT DESIGN ERRORS ADD 282-8,9,10&11, 260-3&4 TDR N001658 1-18-83
C REVISED TO CORRECT DESIGN ERRORS ADDED 276 AND 280 7-18-83
D REVISED TO CORRECT DESIGN ERRORS ADDED 255 RELEASE PER TDR N002763 8-11-83
P1
P2
Z12 8T125
Z36 74LS240
Z24 74LS240
Z11 74LS682
Z59 157
Z48 8T125
Z84 74LS240
Z72 74LS240
Z61 240
Z49 240
Z15 240
Z3 374
Z67 374
Z50 374
Z2 245
Z14 244
Z75 74F574
Z65 74LS245
Z28 PAL16L8 ACN
Z83 PAL16L8 ACN
Z30 PAL16C1
Z63 IMS1421
Z64 PAL16L8 ACN
Z32 74LS240
Z33 74LS175
Z23 74LS240
Z34 74LS175
Z46 74F374
Z16 74LS240
Z9 74LS240
Z8 74LS240
Z6 74LS240
Z47 74LS245
Z17 74LS240
Z42 74LS273
Z54 74LS374
Z40 74LS273
Z66 74LS273
Z27 74LS244
Z43 74LS273
Z26 74LS374
Z38 74LS374
Z29 74LS245
Z31 74LS245
Z45 74LS245
Z25 74LS279
Z37 74LS273
Z39 245
Z51
Z41 74LS138
Z5 74LS85
Z21
Z13
Z22
Z18
Z19
Z20
Z35
Z44
Z52
Z53
Z58
Z61 74F74
Z62 74F74
Z76 74F74
Z77 74F74
Z78 74F74
Z79 74F74
Z80 74F74
Z81 74F74
Z82 74F74
Z74 74F74
CRWEN1
CRWEN2
SRES-
ACLK
SREG-
WERR2-
WERI-
WERO-
SR/W-
SBADR
TBADR-
DEBUG
GDBG
NOTES
1. P1,P2 +5V = 1C,32A
P1,P2 GND = 1A,3A,8A,13A,18A,23A,28A,5C,10C,15C,20C,25C,30C,32C.
2. J2 +5V = 42 44 45 46 47 48
GND = 2-36 EVEN, 40, 50-60 EVEN
3. C20,C21 = 470 uf 10V
C1 THRU C19 = .01 uf 50V
4. J1 GND = PINS 2 THRU 50 EVEN NO'S ONLY
5. DENOTES SPARE
6. REF ASSY PS07-D060
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX = ±.03 .XXX = ±.010 ANGLES ±30'
DASH NO. NEXT ASSY USED ON
APPLICATION
AUTHORIZATION NO.
DR BY R JEFFRIES 1-21-83
CHK BY
APPD BY
APPD BY
PROPRIETARY INFORMATION Rockwell International Corporation NO DISSEMINATION OR USE ALLOWED WITHOUT PRIOR WRITTEN PERMISSION
ROCKWELL INTERNATIONAL CORPORATION Electronic Devices Division 4311 Jamboree Road, Newport Beach, CA 92663
SCHEMATIC DIAGRAM PMC MODULE RDC
SIZE E FSCM NO. 34576 DRAWING NO. PS07-X063
SCALE SHEET 1 OF 1
PS07-2063 D

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE / APPROVED
		TDR N00804 INITIAL RELEASE	
	A	1. ADDED R26-3 TO XZ2-2. 2. ADDED R26-4 TO XZ2-88. 3. R26-3 & -4 WERE SPARES EFFECTIVITY: NONE TDR N003275	10-31-83 Z. BROWN

RELEASED
TO ENGINEERING RECORDS
OCT 07 1983

J1
59 IRQ 9
57 RES 10
55 NMI 11
53 RDY 12
51 S.O. 13
49 Ø2 14
43 R/W 15
41 SYNC 16
39

RZ1 43Ω, TYP
RZ2 43Ω, TYP
RZ3 43Ω, TYP

31 UA15 9 — A15
29 UA14 10 — A14
27 UA13 11 — A13
25 UA12 12 — A12
23 UA11 13 — A11
21 UA10 14 — A10
19 UA9 15 — A9
17 UA8 16 — A8

15 UA7 9 — A7
13 UA6 10 — A6
11 UA5 11 — A5
9 UA4 12 — A4
7 UA3 13 — A3
5 UA2 14 — A2
3 UA1 15 — A1
1 UA0 16 — A0

Z3 (74LS374) OUT EN, CLK
Z2 (74LS374) OUT EN, CLK
Z4 (PAL 16C1)

42 +5V
44
45
46
47
48

38 SCOPE SYNC 1
49 SCOPE SYNC 2
35 HLT CLK
37 WENBI

J2
1 VCC → XZ1-8
5 +5V
6
2
3
4
C7 100µf 16V
C8-C22 .1µf 50V

Z1 (74LS38)
CR1 (IN4148)
CR2 (IN4148)
RZ4 3.3K, TYP
R1 100 1/2W
J4 J3 J5

Z5 (74F244)
Z6 (74F244)
Z7 (74F244)
Z8 (PAL 20L10)
Z9 (74265)
Z10 (74S74)
Z11 (74F245)
Z12 (74F245)
Z13 (74F245)

E1 E2 E3 E4 E5 E6 E7 E8 E9

Q1 (2N2907)
Q2 (2N2222)
R2 270
R3 510
R4 390
R5 390
R6
R7 47K
R8 56K
C1 1000pf 50V
C2 1µf 50V
C3 100pf 50V
C4 220pf 50V
C5 10pf 50V
C6 33pf 50V
Y1
Y2
C24 18pf 50V
C23 18pf 50V
RZ5 1K, TYP
RZ6 10K
RZ5 1K

XZ1
XZ2
XZ3
XZ4
XZ5

J6
7 WENBI
15 HLT CLK
35 FJ
5 2ACLK
3
29 EXTRIG
21 $FFFB-$FFFD
37 UØ2
3 R/W
13 USYNC
59 INTMEM
17 TRACE DBW
31 FJ
9 DISABLE
11 BDBE
1 UR/W
33 NMI
25 RES
51 D7
39 D6
41 D5
43 D4
45 D3
47 D2
49 D1
53 D0
27 ŪRES
23 S̄RES
19 ŪNMI

BSYNC 7
BØ2 39
VCC 8
XTLI 37
XTLO 35
ML 5
UD7 26
UD6 27
UD5 28
UD4 29
UD3 30
UD2 31
UD1 32
UD0 33
IRQ 4
RDY 2
S.O. 38
XZ2 1 21
DBE 36
BUR/W 34
URES 40
UNMI 6

Jumpers
XZ3 1 2 3 4 5 6 7 8
XZ5 1 2 3 4 5 6 7 8 — 28 27 26 25 UD0 24 UD1 23 UD2 22 UD3 21 UD4 20 UD5 19 UD6 18 UD7 17 BA11 16 BA10 15 BA9
XZ4 1 2 3 4 5 6 7 8 — 28 27 26 25 UD0 24 UD1 23 UD2 22 UD3 21 UD4 20 UD5 19 UD6 18 UD7 17 BA12 16 BA11 15 BA10

XZ1-2 J2-1 VCC
XZ1 25 A15 24 A14 23 A13 22 A12 20 A11 19 A10 18 A9 17 A8
XZ1 16 A7 15 A6 14 A5 13 A4 12 A3 11 A2 10 A1 9 A0
XZ1 26 D7 27 D6 28 D5 29 D4 30 D3 31 D2 32 D1 33 D0
XZ1 IRQ 4, RES 40, NMI 6, RDY 2, S.O. 38, Ø2 39, R/W 34, SYNC 7

Z11 D7 18 D6 17 D5 16 D4 15 D3 14 D2 13 D1 12 D0 11 — 2 UD7 3 UD6 4 UD5 5 UD4 6 UD3 7 UD2 8 UD1 9 UD0
Z11 DBDIR 1, DBEN 19, 10

Z13 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7 A6 8 A7 9 — 18 BA0 17 BA1 16 BA2 15 BA3 14 BA4 13 BA5 12 BA6 11 BA7
Z13 DIR 1, 10, 19

Z12 A8 3 A9 2 A10 5 A11 4 A12 7 A13 6 A14 9 A15 8 — 17 BA8 18 BA9 15 BA10 16 BA11 13 BA12 14 BA13 11 BA14 12 BA15
Z12 DIR 1, 10, 19

Z8 (74S38) 1 2 3 — 6 5 4

RZ4 3.3K
RZ5 1K
RZ6 10K
RZ24 3.3K
RZ25 1K
RZ26 10K

SPARES

NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
(2) PINS 2 THRU 36 EVEN, 40 AND 50 THRU 60 EVEN ARE GND ON J1.
(3) PINS 2 THRU 60 EVEN ARE GND ON J6.

PARTS LIST

QTY REQD	QTY REQD	QTY REQD	QTY REQD	QTY REQD	MEAS UNIT	ITEM NO.	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	ZONE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS XX = ± .03, XXX = ± .010; ANGLES ± 30'
MATERIAL:
HEAT TREAT
FINISH

AUTHORIZATION NO.
DR BY G.R. LUTHER 5-4-83
CHK BY 3.9.83
APPD BY E.S. Brandt 10-7-83
APPD BY

ROCKWELL INTERNATIONAL CORPORATION
Electronic Devices Division
4311 Jamboree Road, Newport Beach, CA 92663

SCHEMATIC- R65XXX
EMULATION BOARD No. 1

SIZE E | FSCM NO. 34576 | DRAWING NO. P507-X036 | SHEET 1 OF 1
SCALE

DASH NO. | NEXT ASSY | USED ON
APPLICATION

PROPRIETARY INFORMATION
Rockwell International Corporation
NO DISSEMINATION OR USE ALLOWED WITHOUT PRIOR WRITTEN PERMISSION

P507-X036 A

RELEASED
TO ENGINEERING RECORDS
JUL 14 1983 BY

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	NC	INITIAL RELEASE REL TDR: N002583	5-25-83	

J5: V+USER 1, GND 2, GND 3, +5V 4, +5V 5, GND 6
E1 A B
C5 .001 GND
C6 1uf C1 100uf +5V
R1 1.47K 1/8W 1%
R2 3.57K 1/8W 1%
R3 1.8K +5V +5V
Z19 LM393 2.5v NOMINAL
Z20 MC1403U +5V
Z12 74F74 CLR PR D Q
UPWRDWN
Z11 74F244 TO RZ3-10
TRACE DBW TO J6-17
J1: 1 GND, 3 GND, 5 GND, 7 +5V, 9 +5V, 11 +5V, 13 +5V, 15 +5V, 17 TO J6-59
RZ1 43Ω
Z1 BT125 DIR G
A1 B1 TO Z2-18
A2 B2 TO Z2-16
A3 B3 TO Z2-14
A4 B4 TO Z2-12
A5 B5 TO Z2-9
A6 B6 TO Z2-7
A7 B7 TO Z2-5
A8 B8 TO Z2-3
Z4 74LS14
Z10 74LSØØ
Z13 74LSØØ
Z7 74LS02
Z21 74FØØ
FJ
TO J1-49 DISABLE RES
Z3 74F74 PR D Q CLR
NMI INTSEQ
Z8 74LS02
J6: TO Z10-3 1 URW; TO J1-17 59 INTMEM; TO Z4-5 37 UØ2; 3 R/W; TO Z4-6 55 Ø2; 27 URES; 9 DISABLE; 31 FJ; 21 FFF8-FFFD; TO Z8-4 23 SRES; 25 RES; 29 EXTRIG; 15 HLTCLK; 11; TO Z1-1 17 TRACE DBW; TO Z4-13 19 UNMI; 13 UBSYNC; 5 2ACLK; 7 WENBI; TO Z15-13 33 NMI; 35 FJ; 53 IDØ; 45 ID1; 47 ID2; 49 ID3; 43 ID4; 41 ID5; 39 ID6; 51 ID7
INT MEM 17 — TO J6-59
TARGET WRITE 19
BCSU 21
CLR NMI 23
NMI BREAK 25
SRES 27
FJ BREAK E 29
DISABLE 31
ACLK 33
EXTRIG 35 — TO J6-29
UVCC DWN 37
PENDING NMI 39
IO/M 41
DBE 43
PS2 45
PS3 47
DISABLE RES 49
Z10 74LSØØ UR/W TO J6-1
Z16 74FØØ TO Z6-10
Z11 74F244
SRES
Z9 74F74 PR CLR
TO Z16-13
TO Z18-13
+5V.
Z13 74FØØ
Z15 74LSØ2
Z16 74FØØ
DISABLE
Z15 74LSØ2 13 NMI TO J6-33
Z8 74LSØ2 SRES TO J6-23
Z6 74F08
PENDING NMI
Z14 74LS74 +5V
UNMI
UØ2
Z16 74FØØ
Z5 74LS74
TO Z6-37
TO J6-19
TO J6-55
Z4 74LS14
TO J6-11
Z17 74LS161 A B C D EP ET LD QA QB QC QD
Z13-10
Z21-1
SYNC Ø2
Z7 74LSØ2
TO RZ3-9
SNMI BREAK
SET NMI
CLR NMI
Z6 74F08
TO Z2-17 DB
Z5 74LS74
TO Z3-13
Z10 74LSØØ
Z8 74LS02
Z16 74FØØ
FJ BREAK E
SNI BREAK
TO Z9-2
SYNC
Z9 74F74
Z18 74LS161 CLR QB LD
TO Z13-13
TO J1-35
RZ3
TO Z11-13
TO Z1-1
TO Z4-13
2ACLK
WENBI
TO Z15-13
Z2 74F244 1G 2G 1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4 1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
Z1-18 Z1-17 Z1-16 Z1-15 Z1-14 Z1-13 Z1-12 Z1-11
Z17-14 QA Z13 74FØØ
Z17-13 QB Z21 74FØØ
TO Z6-1
RZ3 43Ω
TO Z11-12
TO Z11-16
RZ2 4.7K +5V
DISABLE RES Z21-13
SPARES Z19 LM393 RZ3 Z11 74F244 Z21 74FØØ

NOTE:
1. ALL EVEN PINS ON J1 & J6 ARE GND.
2. USE .001 uF CAP AS SHOWN IN IC CHART.

IC -	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13	Z14	Z15	Z16	Z17	Z18	Z19	Z20	Z21	RZ1	RZ2	RZ3
VCC	20	20	14	14	14	14	14	14	14	14	20	14	14	14	14	14	16	16	8	1	14	—	1	—
GND	10	10	7	7	7	7	7	7	7	10	7	7	7	7	7	8	8	4	3	7	—			—
CAP	C2	C3	—	C12	—	C4	C13	—	—	C7	C8	—	C14	C9	—	—	C10	C11	—	C15	—	—	—	—

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'
MATERIAL:
HEAT TREAT
FINISH
DASH NO. | NEXT ASSY | USED ON | APPLICATION
AUTHORIZATION NO.
DR BY M. Roe 5-25-83
CHK BY E.S. 7-8-83
APPD BY
APPD BY

PART NO.
ROCKWELL INTERNATIONAL CORPORATION
Electronic Devices Division
4311 Jamboree Road, Newport Beach, CA 92663
SCHEMATIC R65XX
EMULATION POD #2
SIZE D | FSCM NO. 34576 | DRAWING NO. PS07-X041
SCALE Ø | SHEET 1 OF 1
183-G-15 REV. 7/78
NB 3 MX EP 1 T/E
PS07-X041 NC

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